DOCUMENT NUMBER AND REVISION

VL-FS-BTHQ 22008VSS-02 REV. A

(BTHQ 22008VSS-STF-06-LED04YG)

DOCUMENT TITLE:

SPECIFICATION

OF

LCD MODULE TYPE

CUSTOMER	**DATA MODUL**
MODEL NUMBER	**BTHQ 22008VSS-02**
CUSTOMER APPROVAL	
DATE	

DEPARTMENT	NAME	SIGNATURE	DATE
PREPARED BY	PHILIP CHENG	[signature]	2002.11.12
CHECKED BY	M.Y.LU	Lu Min Yuan.	2002. 11. 12
APPROVED BY	CYRUS CHEUNG	[signature]	2002/11/12

DISTRIBUTION LIST: MARKETING

DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2002.11.12	First Release.	PHILIP CHENG	M.Y.LU

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Specification
of
LCD Module Type
Item No.: BTHQ 22008VSS-02

1. General Description

- 20 characters (5x8 dots) x 2 lines STN Positive Yellow Transflective Dot Matrix LCD module.
- Viewing Angle: 6 O'clock direction.
- Driving scheme: 1/16 Duty, 1/5 bias.
- 'SAMSUNG' KS0070BP-00CC (Die form) LCD Controller & Driver or equivalent.
- 'SAMSUNG' KS0065B-PCC (Die form) LCD Segment Driver or equivalent.
- Yellow-green LED04 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	146.0(W) x 43.0(H) x 15.0 MAX.(D)	mm
Effective viewing area	123.0(W) x 23.0(H)	mm
Display format	20 characters x 2 lines	-
Character size	4.840(W) x 9.217(H) (5 x 8 dots)	mm
Character spacing	1.160(W) x 0.536(H)	mm
Character pitch	6.000(W) x 9.753(H)	mm
Dot size	0.956(W) x 1.139(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.971(W) x 1.154(H)	mm
Weight:	Approx. 82	grams

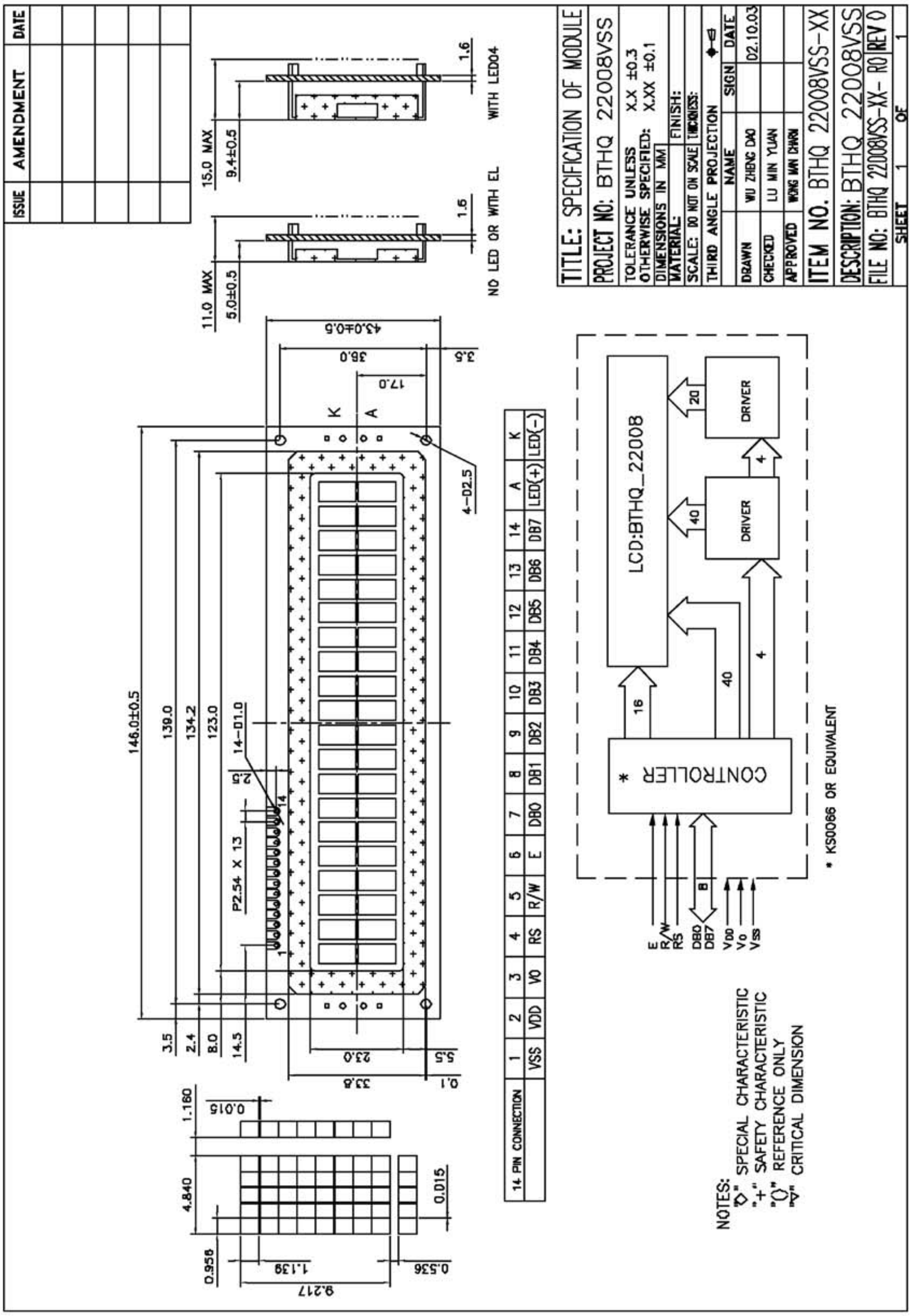


Figure 1: Outline Drawing

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	VSS	Ground(0V).
2	VDD	Power supply for logic (+5V)
3	V0	Power supply for LCD driver
4	RS	Register Select Input: “High” for Data register (for read and write) ”Low” for Instruction register (for write), Busy flag, address counter (for read)
5	R/W	Read/Write signal: ” High” for Read mode. “Low” for Write mode.
6	E	Enable. Start signal for data read /write.
7	DB0	Data input/output (LSB)
8	DB1	Data input/output
9	DB2	Data input/output
10	DB3	Data input/output
11	DB4	Data input/output
12	DB5	Data input/output
13	DB6	Data input/output
14	DB7	Data input/output (MSB)
A	LED(+)	Anode of LED backlight.
K	LED(-)	Cathode of LED backlight.

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 ºC)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD=VDD – V0	-0.3	+15.0	V
Input voltage	Vin	-0.3	VDD +0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.75	5.0	5.25	V
Supply voltage (LCD)	VLCD =VDD-V0	VDD =5.0V, Note1.	4.2	4.6	5.0	V
Input signal voltage for E,DB0-DB7,R/W,RS.	V_{IH}	"H" level	2.2	-	VDD	V
	V_{IL}	" L" level	-0.3	-	0.6	V
Supply Current (Logic & LCD)	IDD	Character mode, Note 1	-	1.4	2.1	mA
		Checker board mode, Note 1	-	1.9	2.9	mA
Supply Current (LCD)	I0	Character mode, Note 1	-	1.0	1.5	mA
		Checker board mode, Note 1	-	1.0	1.5	mA
Supply voltage of yellow-green LED04 backlight	VLED	Forward current =270mA Number of LED dies =2x27 =54.	3.9	4.1	4.3	V

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

At Ta = 0 °C To +50 °C , VDD = +5V±5%, VSS = 0V.

Refer to Fig. 2, the bus timing diagram for write mode.

Table 6

Parameter	Symbol	Min.	Max.	Unit	Test pin
E cycle time	t_C	500	-	ns	E
E rise time	t_R	-	25	ns	E
E fall time	t_F	-	25	ns	E
E pulse width (High, Low)	t_W	220	-	ns	E
R/W and RS set-up time	t_{SU1}	40	-	ns	R/W,RS
R/W and RS hold time	t_{H1}	10	-	ns	R/W, RS
Data set-up time	t_{SU2}	60	-	ns	DB0-DB7
Data hold time	t_{H2}	10	-	ns	DB0-DB7

Refer to Fig. 3, the bus timing diagram for read mode .

Table 7

Parameter	Symbol	Min.	Max.	Unit	Test pin
E cycle time	t_C	500	-	ns	E
E rise time	t_R	-	25	ns	E
E fall time	t_F	-	25	ns	E
E pulse width	t_W	220	-	ns	E
R/W and RS set-up time	t_{SU}	40	-	ns	R/W,RS
R/W and RS hold time	t_H	10	-	ns	R/W, RS
Data output delay time	t_D	-	120	ns	DB0-DB7
Data hold time	t_{DH}	20	-	ns	DB0-DB7

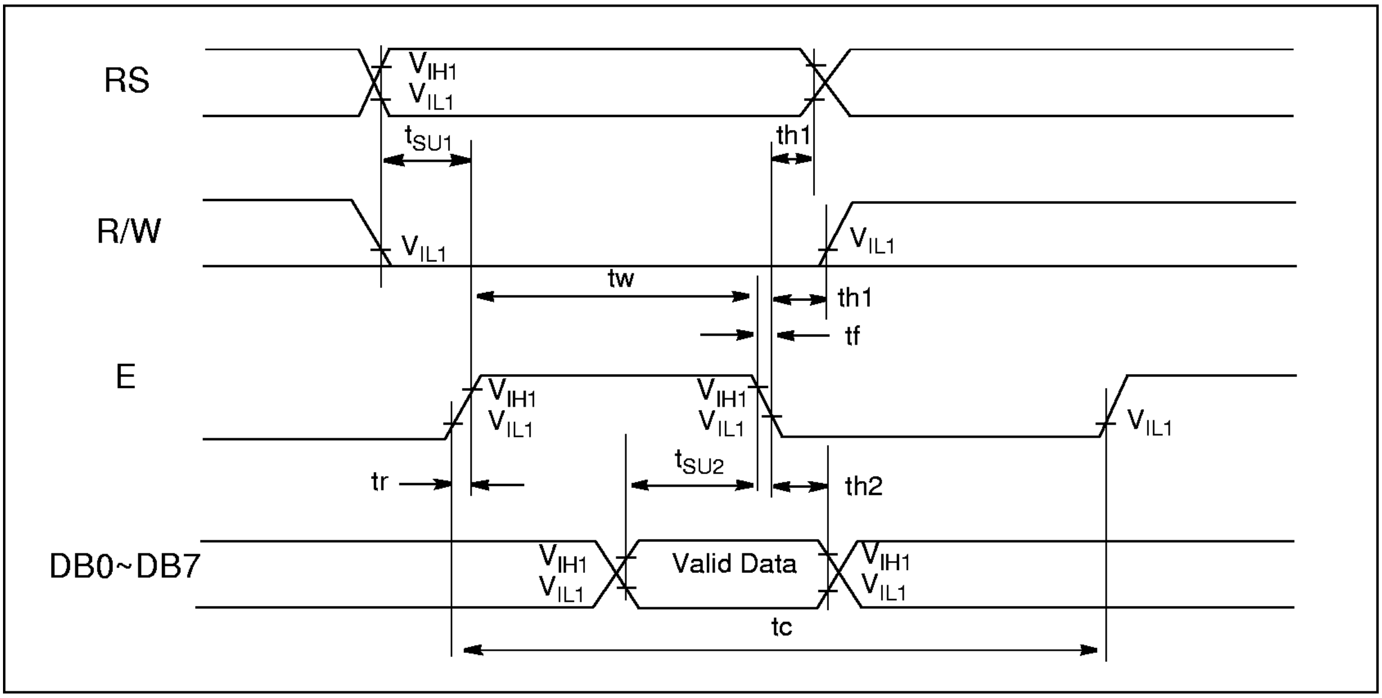


Figure 2: The bus timing diagram for write mode

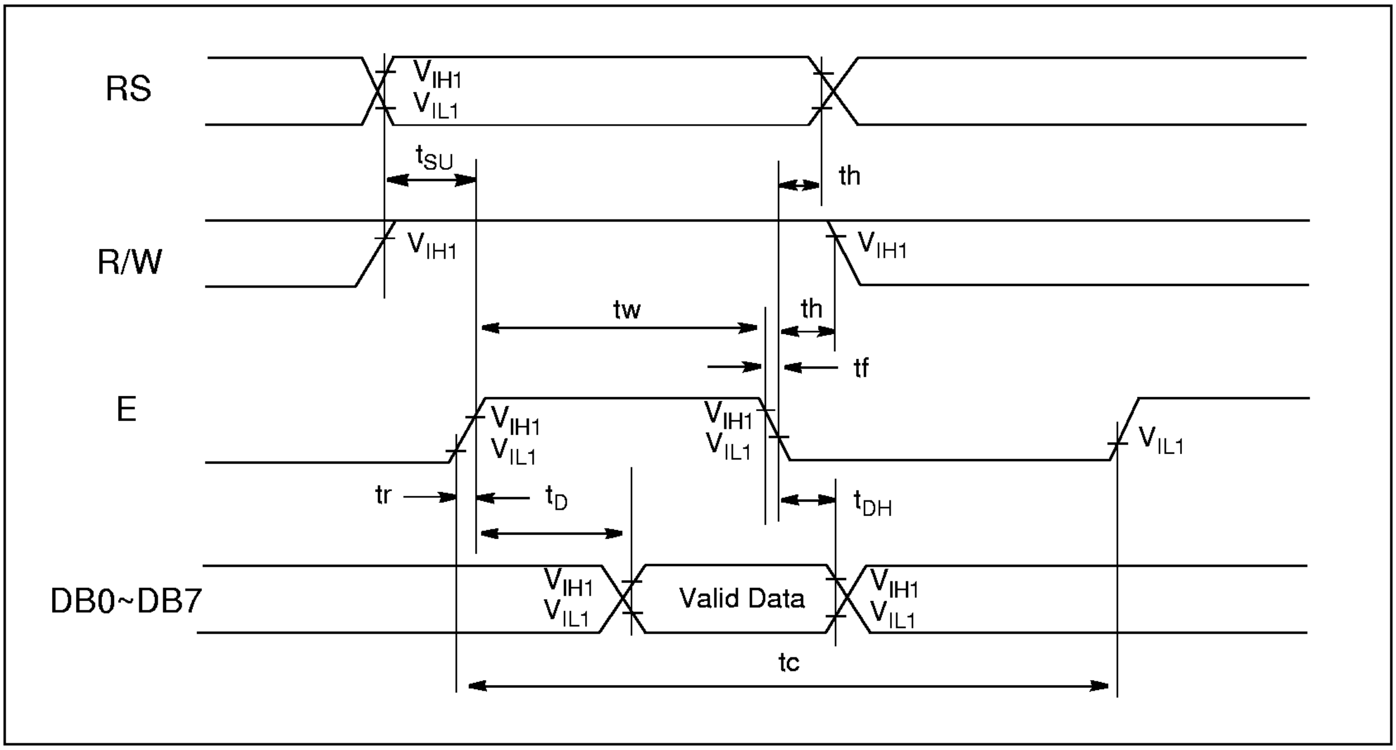


Figure 3: The bus timing diagram for read mode .

5.3 Timing Diagram of VDD against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.

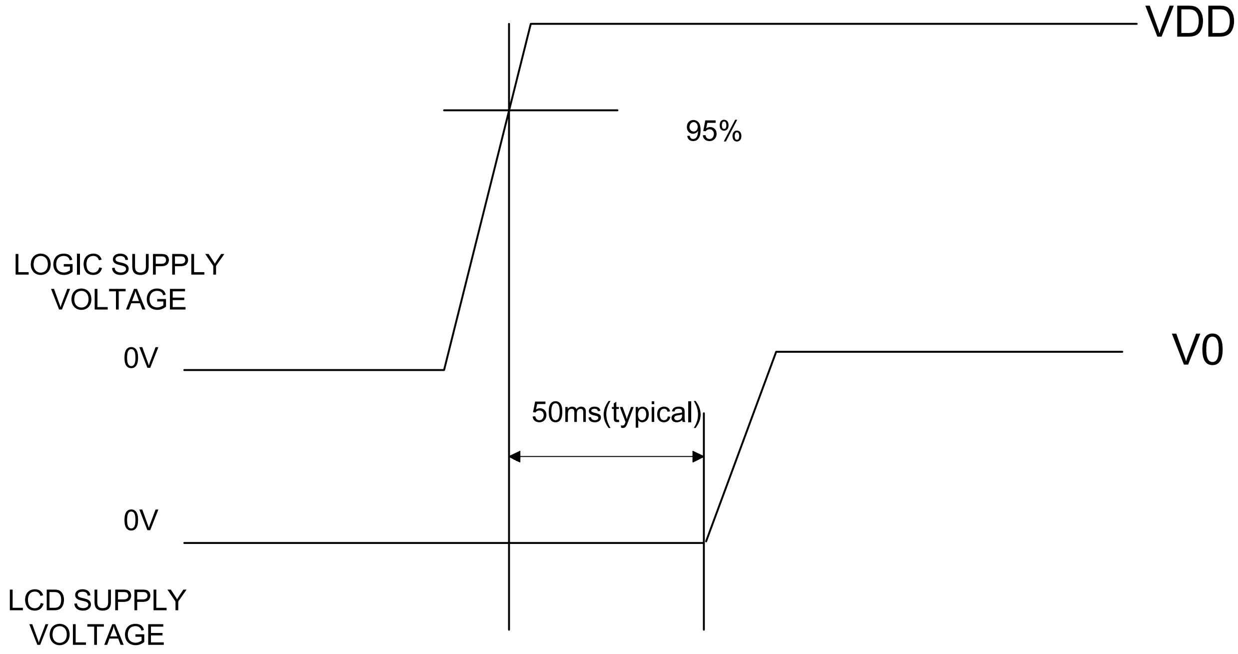


Figure 4: Timing diagram of VDD against V0.

6. CGROM Character Code Table

